

## Claims

5           1. A method for transmitting a debugging information word from a  
computing device, comprising:  
          setting a main processor to run in a debugging mode;  
          said main processor transmitting said debugging information word to a  
keyboard controller; and

10           transmitting, by said keyboard controller, said debugging information  
word using a secondary bus coupled to said keyboard controller.

          2. The method of claim 1, wherein said keyboard controller and said  
main processor communicate by way of a main processor bus.

15           3. The method of claim 1, wherein said secondary bus is an inter-  
integrated circuit bus.

20           4. The method of claim 1, wherein said secondary bus also  
communicates with a battery that provides electrical power to said main  
processor.

25           5. The method of claim 1, wherein said main processor transmits  
debugging information words to said keyboard controller only when said main  
processor operates in said debugging mode.

          6. The method of claim 1, additionally comprising receiving, by a  
converter interfaced to said secondary bus, said debugging information word  
transmitted from said keyboard controller.

30           7. The method of claim 6, additionally comprising said converter  
transmitting said debugging information word to an external receiver.

8. The method of claim 1, wherein said debugging mode is a kernel mode of an operating system.

5 9. A computer that is debugged by way of a connection to a secondary bus, comprising:

a main processor that executes an operating system program in a kernel mode;

10 a keyboard controller that interfaces to said main processor, said keyboard controller communicating debugging information words with said main processor; and

a secondary bus that interfaces with said keyboard controller, said secondary bus being used to convey said debugging information words.

15 10. The computer of claim 9, wherein said secondary bus does not interface directly with said main processor.

20 11. The computer of claim 9, wherein said secondary bus interfaces with an adapter that receives said information words from a computing device external to said computer.

25 12. The computer of claim 9, wherein said main processor receives debugging information words from said keyboard controller only when said main processor operates in said kernel mode.

13. The computer of claim 9, wherein said main processor transmits debugging information words from said keyboard controller only when said main processor operates in said kernel mode.

30 14. The computer of claim 9, wherein said secondary bus interfaces to a module that supplies electrical power to said main processor.

15. The computer of claim 9, wherein said secondary bus is an inter-integrated circuit bus.

16. A method for receiving a debugging information word by a main processor, comprising:  
5        setting said main processor to run in a debugging mode;  
         receiving, by a keyboard controller coupled to said main processor, said debugging information word from a secondary bus; and  
         said keyboard controller transmitting said debugging information word to  
10        said main processor.

17. The method of claim 16, wherein said keyboard controller and said main processor communicate by way of a main processor bus.

18. The method of claim 16, wherein said secondary bus is an inter-integrated circuit bus.

19. The method of claim 16, wherein said main processor receives debugging information word from said keyboard controller only when said main processor operates in said debugging mode.

20. The method of claim 16, additionally comprising receiving said debugging information word from an adapter that transmits said debugging information word along said secondary bus wherein said adapter interfaces with  
25        an external source.

21. One or more computer-readable media having computer-readable instructions thereon which, when executed by a computer, cause the computer to perform a method for receiving a debugging information word by a main processor comprising the steps of:

         setting an operating system that runs on said main processor of said computer to run in a kernel mode;

receiving, by a keyboard controller coupled to said main processor, a debugging information word from a secondary bus; and

transmitting, by said keyboard controller, said debugging information word to said main processor.

5

22. The method of claim 21, wherein said keyboard controller and said main processor communicate by way of a main processor bus.

23. The method of claim 21, wherein said secondary bus is an integrated circuit bus.

10

24. The method of claim 21, wherein said main processor receives debugging information words from said keyboard controller when said main processor operates in said debugging mode.

15

25. The method of claim 21, additionally comprising receiving said debugging information word from an adapter that transmits said debugging information word along said secondary bus wherein said adapter interfaces with an external source.

20

26. A system for debugging a first computer by way of a second computer, the system comprising:

a main processor that operates in said first computer, said main processor executing an operating system program that runs in a kernel mode;

25

a keyboard controller that interfaces with said main processor, said keyboard controller communicating debugging information words with said main processor;

a secondary bus that interfaces with said keyboard controller, said secondary bus being used to convey said debugging information words; and

30

an adapter that conveys said debugging information to said second computer, wherein said second computer is interfaced to said first computer by way of said secondary bus.

27. The system of claim 26, wherein said secondary bus additionally communicates with a battery module of said first computer.

5           28. The system of claim 26, wherein said secondary bus additionally communicates with at graphical pointing device.

10           29. The system of claim 26, wherein said secondary bus additionally communicates with at least one indicator that presents information as to the status of said first computer.

10011308 20030606